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# Reappraisal of Clock Gating Methods in Different Conditions

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**Abstract**: Nowadays digital concept is used in all fields; every multimedia and DSP based devices are clock based synchronous and asynchronous devices. Clock signals with large frequency are on demand but as frequency of clock increases, power consumption of modules also increases, since power dissipation is directly related to clock frequency. Clock gating method is used to reduce dynamic power, which is due to clock frequency. In this paper review of existing clock gating methods is performed at 90nm technology with different frequency and voltage by applying it on synchronous design like 16-bit FIFO. The proposed architecture is designed using verilog language. The synthesis and simulation work is performed in Xilinx ISE Design suite 14.2 tool and power analysis is done by XPOWER ANALIZER.

**Keywords**: DSP, Clock gating, Power dissipation, 16-bit FIFO.

## I. INTRODUCTION

As technology is growing, number of transistors in a unit area is increasing so; power consumption of circuit is also increasing. But today power has become a prime factor, and is critical in battery operated portable devices. Clock signal is a great source of power dissipation because of high frequency of operation. Increased power consumption is main obstacle in the realization of high performance design. Energy efficient devices and optimized power devices are on demand. With the popularity of portable battery operated digital devices and mobile applications, optimization of power is needed. In order to achieve a design with optimized power, designers go through several iterations. In order to achieve high performance and high integration density, semiconductor devices are continuously scaled in each technology generation. Because of increased density of transistors and higher operating frequency, the power consumption in a die is increasing with every technology generation.

Clock signals are only means of synchronization, it does not contain any information. Clock signals provide timing references for various operations in a synchronous digital system. This clock signals are responsible for 50-70 percent of total chip power and it increases in the next generation of designs [5].

In this paper, previous work will be discussed. After that power dissipation in a VLSI circuit is presented and then techniques for reduction of Dynamic power are discussed. Existing clock gating technique is applied on 16-bit FIFO module and result is studied on 90nm technology and different voltage, frequency and temperature. These all results are compared between without clock gating and with clock gating technique. Finally conclusion is given at last on the paper.

## II. PREVIOUS WORK

Some information related to this paper is fetched from different references. In reference [1] review of existing clock gating methods are available. In this paper RTL Clock gating technique is used to optimize dynamic power. The optimization technique is applied on 8-bit ALU. This RTL approach saves lots of efforts. For reducing dynamic power, RTL clock gating technique finds number of FLIP FLOPs that share a common enable signal, and uses this enable signal to control the clock gating circuit. In reference [2] review of every existing clock gating circuit is presented. Clock gating by AND gate is the simple one, it has two inputs one is global clock and another is enable signal. This enable signal controls the output of AND gate, i.e. it controls the gated clock but it has problem of glitch, which makes it not useful. NOR gate is useful when actions are to be performed on rising edge of the global clock. Latch based clock gating is used to rectify the problem of glitch, 'En' signal is given through latch. MUX based clock gating is simple, robust, compliant and reasonable choice, but it is expensive and has high power consumption and FLIP-FLOP based clock gating is used when falling edge of clock is used for operation but it has a disadvantage of longer sleep period. In reference [3] clock gating technique and dynamic voltage frequency scaling technique is applied in the form of hardware, is presented. Power consumption of CPU with and without clock gating and dynamic voltage frequency scaling is compared by SPICE simulation. Significant reduction in power is obtained. In reference [4] a FLIP-FLOP

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based new clock gating technique is presented to reduce the gating overhead. Some applications like counter and SAR is used to reduce the number of transistors and to achieve more power saving. In reference [5] author presented application of latch free clock gating technique on ITC'99-bo1 standard benchmark circuit and the result is compared on different frequency level as 1GHz, 10GHz, 100GHz and 1THz. In reference [6] encoder, decoder and convertor circuits are designed using clock gating technique which reduces power without degrading system's performance and reference [7] gives knowledge about total power. Total power is sum of dynamic power and leakage power. Dynamic power has two components, one is switching power due to capacitances and another is short circuit power. Various circuit techniques are discussed that are used to maintain power consumption within limit.
According to the previous research background, lots of clock gating techniques are there but still those techniques are not up to the mark due to some issues. All previous clock gating approaches are facing some problems, some have problem of size. Those approaches which require less size are having some problem of glitches and those approaches which are having large size, there is no any glitches problem but those structures are increasing static problem. In all previous approaches, only few approaches have reduced the clock power but still some are facing the problem of clock power [8]. In some previous architecture, there is a need of extra input and output pins and in a VLSI chip, increase in input and output pins will lead to the increase of cost of the whole process.

## III. POWER DISSIPATION IN VLSI

Basically there are two types of power consumption in a circuit one is static power and other is dynamic power. Static power is also called leakage power. Clock gating is mainly used for optimization of dynamic power.

A. Dynamic Power Reduction Techniques
Though the leakage power increases significantly in every generation with technology scaling, the dynamic power still continues to dominate the total power dissipation of the general purpose microprocessors. Effective circuit techniques are available for the reduction of dynamic power dissipation.
Clock gating- Clock gating is an efficient way of power optimization. In a digital circuit clock gating technique is used to reduce dynamic power. In a general synchronous circuit such as general purpose microprocessor, only a portion of circuit works at a given time. Hence by shutting down the unused portion of the circuit, the unnecessary power consumption can be prevented. It can be done by masking the clock that goes to the idle portion of the circuit [7].

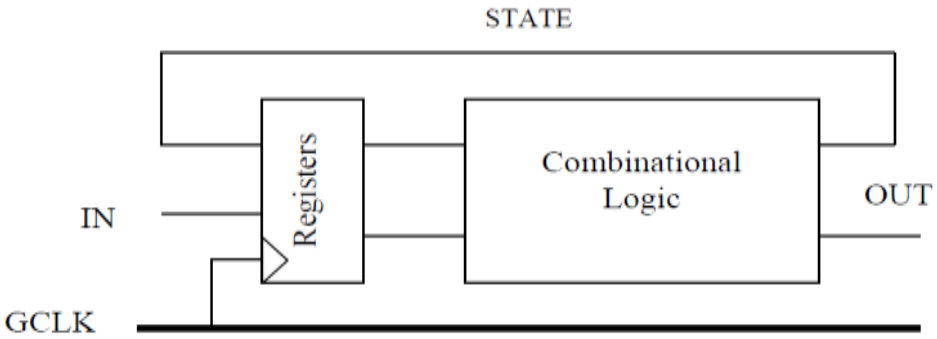


Fig. 1 Single clock, flip-flop-based FSM

By applying this clock gating technique, inputs of unused portion of the circuit block will not change; consequently dynamic power reduction becomes smaller.
In fig. 1 combinational circuit block has two inputs, one is input signal and other is clock signal. Both input and clock signals to the combinational logic block are applied through the registers, which are generally a combination of sequential elements like D- flip-flops [7]. Hence, in the figure 1 clock gating technique is not used, global clock is directly applied to the module, so dynamic power dissipation is high in this circuit.
An optimized power design is implemented in figure 2[7]. In this figure a latch and an AND gate is connected before register module. AND gate has glitch problem, this problem can be eliminated by connecting a latch before AND gate. This latch prevents any glitches in (fa) from propagating to the AND gate when global clock is high. Hence (fa) is used as a control signal to control the operation of combinational block. When (fa) is high, local clock is blocked, at this instant combinational logic does not work, hence dynamic power dissipation has been prevented. The circuit operates as follows.
The signal (fa) is only valid before the rising edge of the global clock. When the global clock is low, the latch is transparent, however, (fa) does not affect the AND gate. If (fa) is high during the low-to-high transition of the global

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clock, then the global clock will be blocked by the AND gate and local clock will remain at low. Power saving efficiency of a clock gating technique stoutly depends on the efficient synthesis and optimization of clock gating module or the module which controls the clock signal.

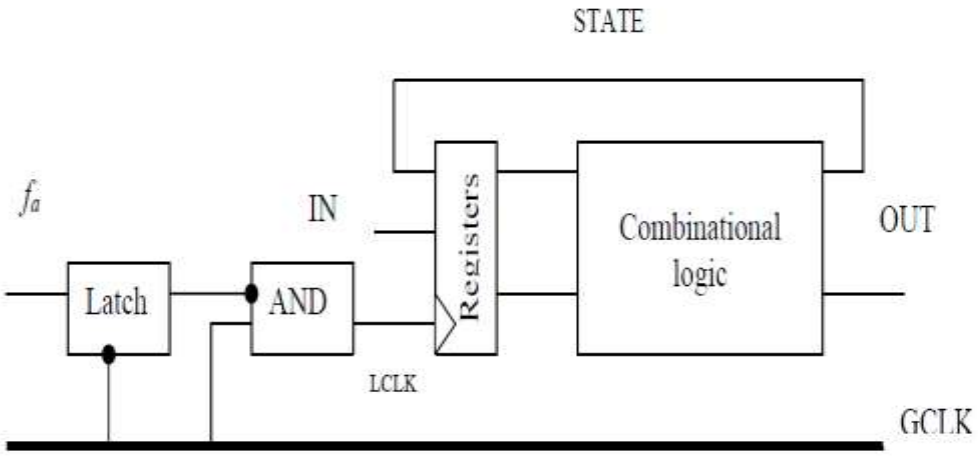



Fig. 2.Schematic diagram of gated clock design

Effective clock gating requires a methodology that determines which circuits are gated, when, and for how long.

B. Implementation Details

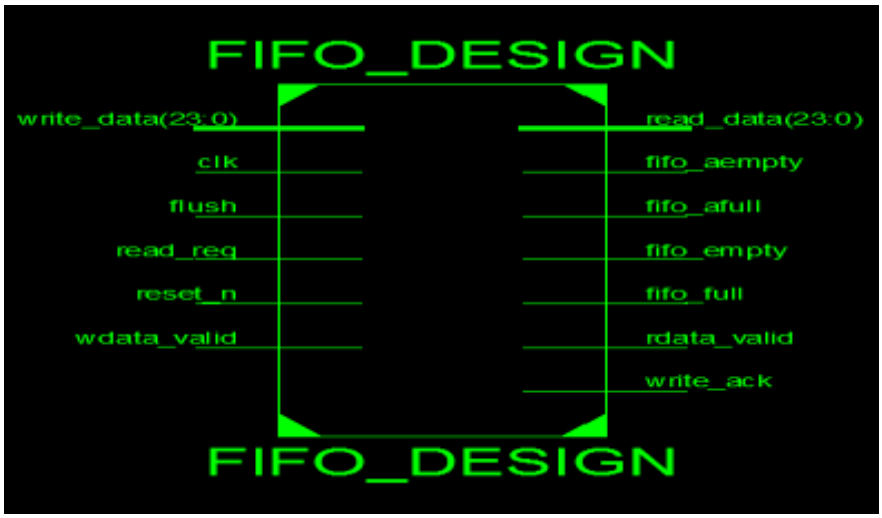
There are following applications of clock gating:

- Clock gating technique is basically used for reduction in dynamic power of all synchronous system like ALU, FIFO and general purpose processors[4-5].
- Clock gating is also used for reduction of clock power, because in all large synchronous system like DSP processors, graphics processors require large clock power. So by using clock gating those clock powers can be reduced.

In this paper 16 bit FIFO synchronous design is used, which is connected to the clock gated circuit. Here power analysis will be done on different parameters like frequency, voltage, 90nm technology. In this work, comparative analysis is done with all existing clock gating approach and try to reduce the clock & dynamic power up to the mark with reduction in clock gating hardware unit size.

## IV. SIMULATION AND RESULT

In this paper, various designs are implemented using different types of clock gating techniques. All the techniques are performed at 90nm technology with different temperature, voltages and frequencies and their dynamic, static and total power has been computed. In this study, clock gating techniques are applied on a 16- bit FIFO.




(a)

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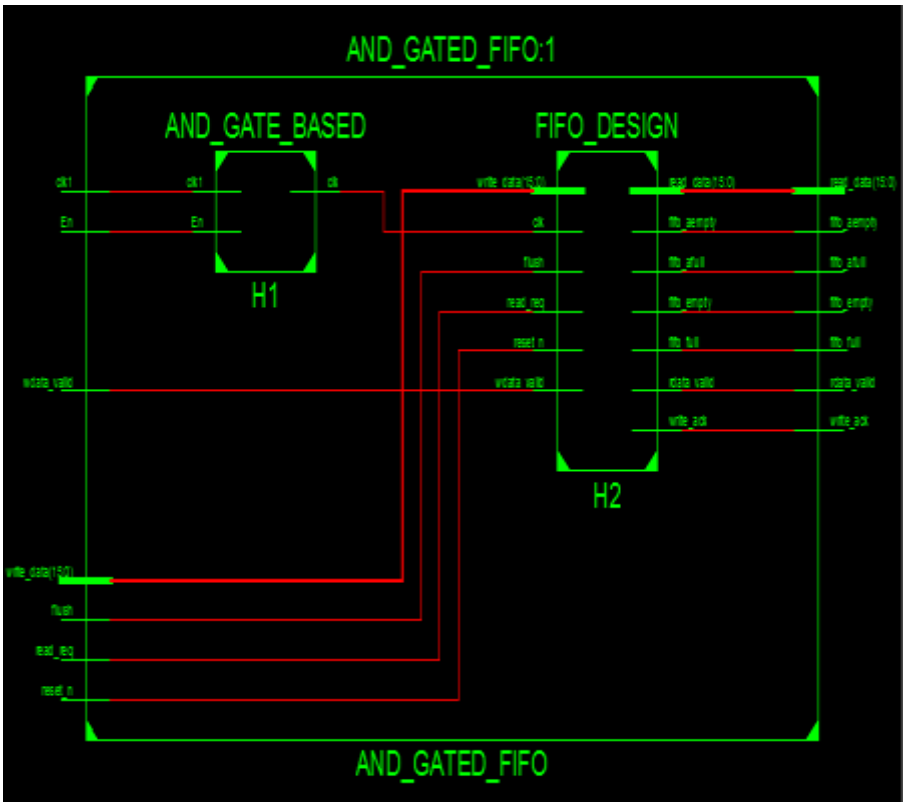


(b)

Fig. 3 (a) Top Module of FIFO using Verilog Design (b) Top Module of FIFO with clock gating using Verilog Design

The existing clock gating techniques are implemented using Verilog HDL. The results are shown in the form of BAR GRAPH. All experiments are done on Xilinx14.2 EDA tool, Mentor Graphics, Model SIM. For power calculation XPOWER is used, Spartan-3(90nm) FPGA platform is used for result and analysis. Voltage and temperature analysis is done at 5GHz and 10GHz.

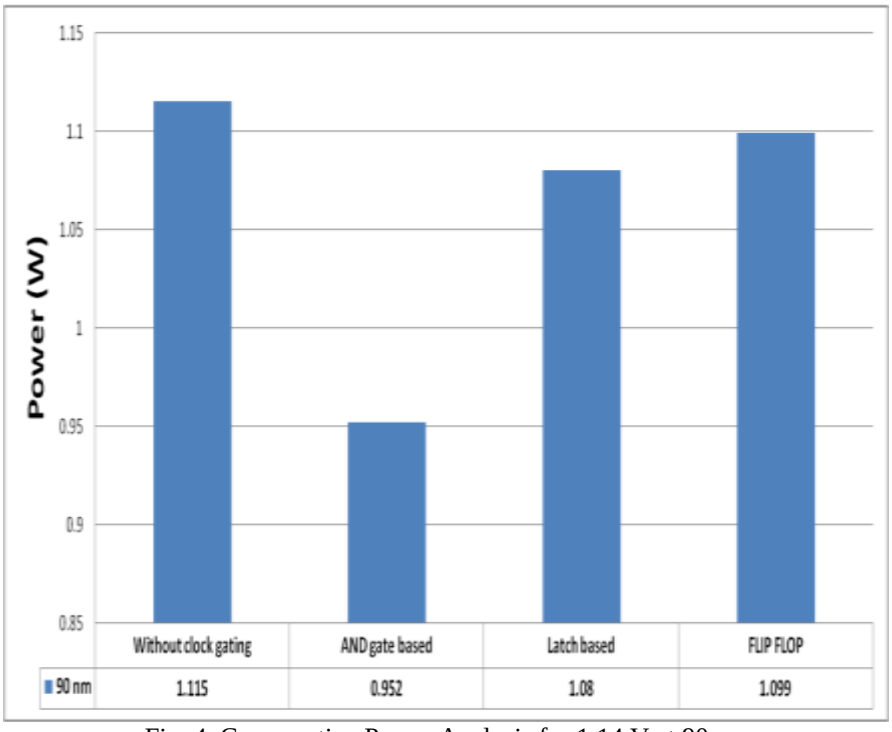


Fig. 4. Comparative Power Analysis for 1.14 V at 90nm


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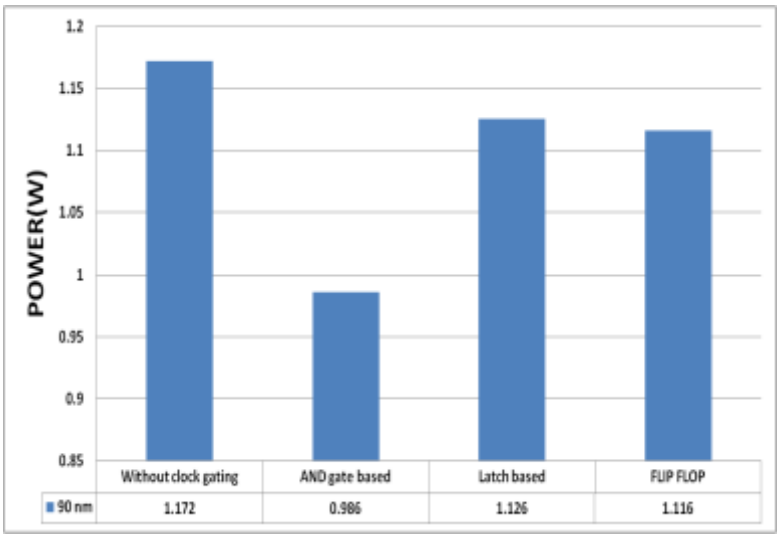


Fig. 5 Comparative Power Analysis for 1.2 V at 90nm

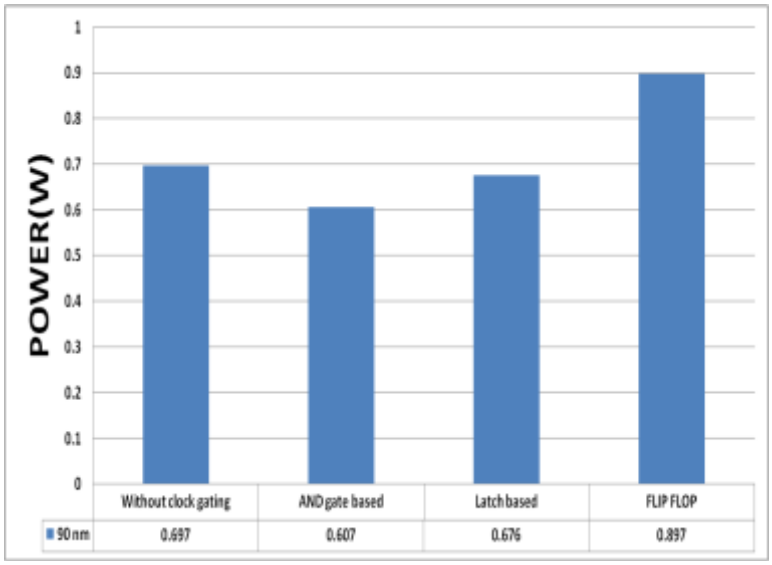


Fig. 6 Comparative Power Analysis for 5GHz at 90nm

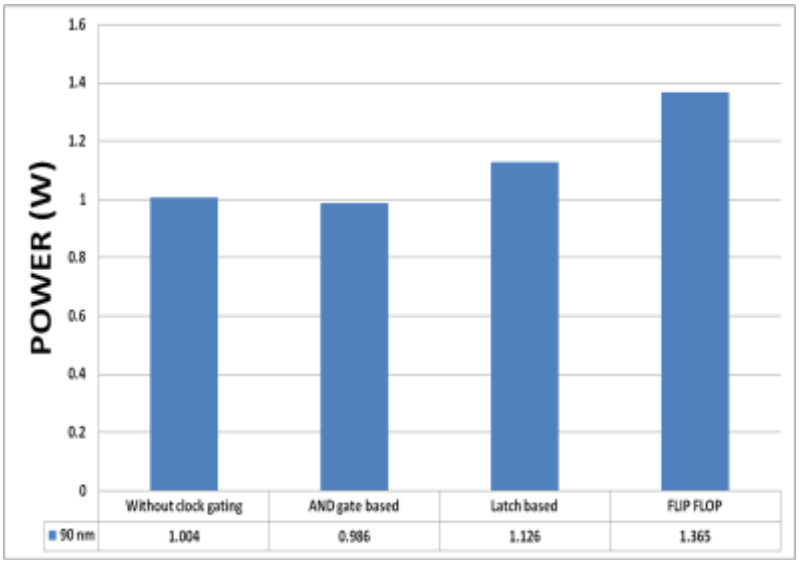


Fig. 7 Comparative Power Analysis for 10GHz at 90nm


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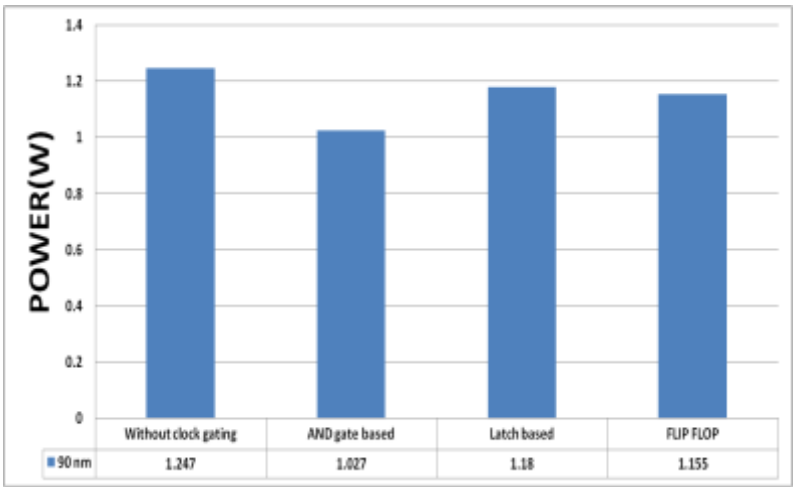


Fig. 8 Comparative Power Analysis for Temp=50, at 90nm

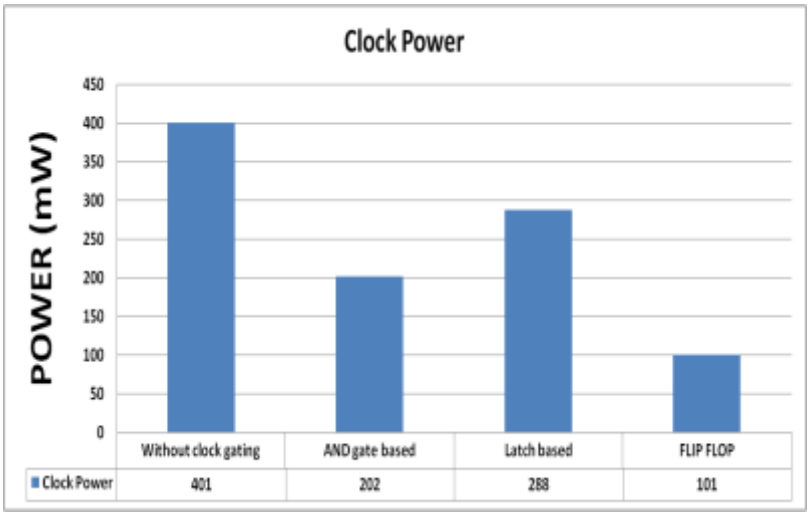


Fig. 9 Comparative Power Analysis for clock power

## V. CONCLUSION

From the above results, it has been observed that the power consumption is low when FIFO is running in Gated clock mode. But every design has an advantage and disadvantage. In terms of area, the AND gated clock consumes less area i.e. only two gates are required and the power consumed is lower than normal FIFO. It can be seen that there is tremendous change in clock power as compared to previous approaches. In terms of clock power, the positive level flip-flop is good but it consumes more area. The glitches and hazards are another issue in these techniques. From the clock power and gate count, it can understood that there is need of a new design low clock power and low area or gate.

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